

01/06/00  
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01-07-00

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THE COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington D.C. 20231  
Box Patent Applications

Case Docket No. FUJA 16.923  
Filed by Express Mail  
(Receipt No. EL522353992US)  
on January 6, 2000  
pursuant to 37 CFR 1.10  
by [Signature]

Jc684 U.S. PTO  
09/478604  
01/06/00

S I R:

Transmitted herewith for filing is: ☒ a new application  
☐ a e-i-p application of S.N. \_\_\_\_\_ filed \_\_\_\_\_

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For: BURST SIGNAL DETECTION CIRCUIT

Enclosed are:

☒ 23 sheets of drawings (Figs. 1,2A-2C,3A,3B,4,5,6A-6C,7,8,9A-9C,10A,10B,11,12A-12C,  
13-15,16A-16C,17-19,20A,20B,21,22A,22B,23A-23C)

☒ Specification, including claims and abstract ( 46 pages)

☒ Declaration

☒ An assignment of the Invention to FUJITSU LIMITED

☒ A certified copy of Japanese Application No. 11-062290

☒ An associate power of attorney

☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27

☒ Post card

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☐ Information Disclosure Statement, PTO-1449, copies of \_\_\_\_\_ references

☐ Other \_\_\_\_\_

☐ Other \_\_\_\_\_

	Col. 1	Col. 2
FOR:	NO. FILED	NO. EXTRA
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TOTAL CLAIMS	39-20 =	19
INDEP CLAIMS	4-3 =	1
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS PRESENTED		

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BURST SIGNAL DETECTION CIRCUIT

## BACKGROUND OF THE INVENTION

## 5 1. Field of the Invention

The present invention relates to a burst signal detection circuit for detecting the arrival of a burst-like signal, and in particular to a burst signal detection circuit used most suitably for a transmission system for transmitting a high-speed optical burst signal in a system such as a passive optical network (PON) system used in a transmission for optical subscriber system.

## 15 2. Description of the Related Art

In the transmission of an optical burst signal, the timing of sending out the burst signal to be transmitted is not definitely determined, and therefore a burst signal detecting signal is required to notify the arrival of the burst signal to the transmission system.

20 For configuring a flexible network system in which each terminal unit for sending out the burst signal can be accommodated at an arbitrary position on the network and a restriction on the transmission distance is relaxed, it is necessary to accurately discriminate the arrival of a weak burst signal from a remote terminal unit on the one hand and the absence of a burst signal on the other hand.

The present invention relates to a burst signal detection circuit for detecting the arrival of a burst signal at a low level accurately without deteriorating the receiving characteristic. In the prior art, the receiving characteristic may be deteriorated by the DC level fluctuation due to the low-frequency response of a photo-diode (PD) for detecting an optical signal.

35 Fig. 21 shows a configuration of a conventional burst signal detection circuit in a receiver for receiving an optical burst signal. The optical burst

Filed by Express Mail  
(Receipt No. 1522599205)  
on 1/6/00  
pursuant to 37 C.F.R. 1.10.  
by Lozano

signal detection circuit includes a photo-diode (PD) 210 for converting an optical signal into a current signal, a preamplifier 211 for converting the current signal output from the photo-diode (PD) 210 into a voltage signal, a  
5 signal amplifier 213 for amplifying a weak signal output from the preamplifier 211 and producing a sufficiently large logic signal, and an amplitude identifying circuit 215 for detecting the presence or absence of a burst signal based on the signal output from the preamplifier  
10 211.

To process the burst signal, the signal amplifier 213 includes an automatic threshold control (ATC) circuit 214 and a buffer amplifier 213A. The input signal from the preamplifier 211 and a threshold level  
15 from the automatic threshold control (ATC) circuit 214 are differentially amplified by the buffer amplifier 213A thereby to output a received signal.

The automatic threshold control (ATC) circuit 214 includes a peak detection circuit 214A, a bottom  
20 detection circuit 214B, and a voltage dividing circuit 214C. Upon application of a burst signal thereto through the preamplifier 211, the peak detection circuit 214A and the bottom detection circuit 214B instantaneously detect the maximum level and the minimum level, respectively, of  
25 the input signal, and the voltage-dividing circuit 214C sets the central level of the amplitude of the input signal providing the voltage-dividing level as a threshold level and outputs it to the buffer amplifier 213A.

In the amplitude identifying circuit 215, a  
30 peak detection circuit 216A in an amplitude detection circuit 216 detects the peak level of the input signal from the preamplifier 211, and a comparator 215A compares the input peak level with a threshold level and outputs a  
35 burst signal detection signal indicating the presence or absence of the burst signal.

As shown in Fig. 23A, the frequency

characteristic of the conversion efficiency of a photo-diode (PD) used as an element for receiving the optical signal is known to have a "drop" in the range of several to several hundred kHz and the conversion efficiency increases in the low-frequency region.

This phenomenon is considered to stem from the carriers generated by the optical signal entering the regions other than the light detecting surface of the photo-diode (PD) where an electric field is not applied. The carriers, to which the electric field is not applied, move slowly, by diffusion, and therefore have a very large time constant.

The shoulder of the low-frequency response characteristic is very small and, usually, can be ignored. In the case where burst signals having considerably different amplitudes are input continuously to the photodiode, however, the problem described below arises.

Assuming that, as shown in Fig. 23B, a second burst signal (packet #2) of a small amplitude arrives and is received by the photo-diode (PD) immediately after the end of a first burst signal (packet #1) of a large amplitude at an interval of a short guide time  $T_g$ , the current output of the photo-diode (PD) responds to a waveform such that, as shown in Fig. 23C, the DC level (bottom level) thereof gradually rises due to the low frequency response at the time of receiving the first burst signal (packet #1) having a large amplitude and the DC level is restored to the original level at the immediately subsequent time after the first burst signal when the second burst signal (packet #2) is received.

The adverse effect of the DC level variation due to the low frequency response depends on the magnitude of the amplitude of the burst signal. That is, the DC level variation is relatively small for the first burst signal (packet #1) having a large amplitude and therefore has no effect on the detection of the burst

signal. However, the DC level variation is large and is not negligible for the second burst signal (packet #2) having a small amplitude, and has an adverse effect on the burst signal detection.

5           Figs. 22A and 22B show operating waveforms for detecting the burst signal at the time of the leading portion of the second burst signal (packet #2). Fig. 22A shows an input signal (a) of the amplitude identifying circuit 215, a peak detection output (b) of the peak  
10   detection circuit 216A, and a threshold level (c) of the threshold level control circuit 217B.

          The send-out time length of a burst signal is predetermined. A reset signal is generated during the guard time  $T_g$  at predetermined timing, and the peak level  
15   of the peak detection circuit 216A is reset by this reset signal.

          The input signal (a) shown in Fig. 22A is such that the bottom level output from the photo-diode (PD) is increased by the DC component of the burst signal (packet  
20   #1) of a large amplitude that has arrived immediately before. The bottom level of the input signal (a) thus had already exceeded the threshold level (c) at the time of the reset described above. As shown in Fig. 22B, therefore, the comparator 215B outputs a detection signal  
25   (d) erroneously indicating the presence of a burst signal even in the absence of the burst signal.

          Specifically, the problem arises in the case where the waveform moves to the low voltage side due to the variation of the bottom level. That is, in this  
30   case, while the bottom detection circuit can follow the movement of the waveform, however, the peak detection circuit holds the maximum level of the signal, so that it erroneously detects the amplitude of the input signal as a large amount larger than the actual amplitude. Even in  
35   the case where the actual signal is smaller than a specified threshold level or, even worse, in the absence of a signal, a detection signal indicating the presence

of the burst signal is erroneously output.

#### SUMMARY OF THE INVENTION

An object of the present invention is to provide a burst signal detection circuit for detecting a burst signal with high accuracy against the DC level variation attributable to the low frequency response of the photodiode (PD), etc. even in the case where the arriving burst signal is a weak optical signal.

In order to attain the above object, according to the present invention, a DC variation removing circuit is inserted in the stage before detecting the amplitude of the input signal so that the signal input to an amplitude detection circuit develops no DC level variation.

The DC variation removing circuit can be realized by a configuration or a modification thereof in which the output signal of a bottom detection circuit or a peak detection circuit for detecting the DC level variation and the output signal of a preamplifier are differentially amplified.

According to a first aspect of the invention, there is provided a burst signal detection circuit comprising a DC variation removing circuit for detecting the bottom level or the peak level of an input signal and removing the DC level variation of the input signal based on the bottom level or the peak level, and an amplitude identifying circuit for detecting the presence or absence of a burst signal based on the output signal of the DC variation removing circuit, wherein the amplitude signal identifying circuit includes an amplitude detection circuit for detecting the maximum amplitude of the output signal of the DC variation removing circuit, a threshold level control circuit for controlling the threshold level, and a comparator circuit for comparing the output level of the amplitude detection circuit with the threshold level and outputting a detection signal indicating the presence or absence of the burst signal.

According to a second aspect of the invention, there

is provided a burst signal detection circuit comprising a DC variation removing circuit for detecting the bottom level or the peak level of the input signal and removing the DC level variation of the input signal based on the bottom level or the peak level, a signal amplifier for amplifying the output signal of the DC variation removing circuit and an amplitude identifying circuit for detecting the presence or absence of the burst signal based on the output signal of the signal amplifier, wherein the amplitude identifying circuit includes an amplitude detection circuit for detecting the maximum amplitude of the output signal of the signal amplifier, an threshold level control circuit for controlling the threshold level, and a comparator circuit for comparing the output level of the amplitude detection circuit with the threshold level and outputting the detection signal indicating the presence or absence of the burst signal.

According to a third aspect of the invention, there is provided a burst signal detection circuit comprising an amplitude detection circuit for detecting the bottom level or the peak level of the input signal and removing the DC level variation of the input signal based on the bottom level or the peak level while at the same time detecting the maximum amplitude of the input signal, a threshold level control circuit for controlling the threshold level, and a comparator circuit for comparing the output level of the amplitude detection circuit with the threshold level and outputting a detection signal indicating the presence or absence of the burst signal.

According to a fourth aspect of the invention, there is provided a burst signal detection circuit comprising a DC variation removing signal amplifier for detecting the bottom level or the peak level of the input signal and removing the DC level variation of the input signal based on the bottom level or the peak level while at the same time amplifying the input signal, and an amplitude identifying circuit for detecting the presence or absence

of the burst signal based on the output signal of the DC variation removing signal amplifier, wherein the amplitude identifying circuit includes an amplitude detection circuit for detecting the maximum amplitude of the output signal of the DC variation removing signal amplifier, a threshold level control circuit for controlling the threshold level, and a comparator circuit for comparing the output level of the amplitude detection circuit with the threshold level and outputting a detection signal indicating the presence or absence of the burst signal.

According to a fifth aspect of the invention, there is provided a burst signal detection circuit, wherein the DC variation removing circuit includes a bottom detection circuit or a peak detection circuit for detecting the bottom level or the peak level, respectively, of the input signal and a differential amplifier for differentially amplifying the output signal and the input signal of the bottom detection circuit or the peak detection circuit.

According to a sixth aspect of the invention, there is provided a burst signal detection circuit wherein the DC variation removing circuit includes a bottom detection circuit or a peak detection circuit for detecting the bottom level or the peak level, respectively, of the input signal, a level shift circuit for shifting the output signal of the bottom detection circuit or the peak detection circuit by a predetermined value, and a differential amplifier for differentially amplifying the output signal and the input signal of the level shift circuit.

According to a seventh aspect of the invention, there is provided a burst signal detection circuit, wherein the amplitude detection circuit includes a master-slave type amplitude detection circuit configured with a master bottom detection circuit or a master peak detection circuit for detecting the absolute minimum



level or the absolute maximum level, respectively, of the input signal, and a slave peak detection circuit or a slave bottom detection circuit for detecting the relative maximum level or the relative minimum level, respectively, of the input signal from the output level of the master bottom detection circuit or the master peak detection circuit.

According to an eighth aspect of the invention, there is provided a burst signal detection circuit, wherein the master-slave type amplitude detection circuit is so configured that the level-hold capacitor of the slave peak detection circuit or the slave bottom detection circuit is connected to the output of the master bottom detection circuit or the master peak detection circuit.

According to a ninth aspect of the invention, there is provided a burst signal detection circuit, wherein the DC variation removing signal amplifier includes a bottom detection circuit or a peak detection circuit for detecting the DC level variation of the input signal, and an amplifier supplied with the same input signal and the output signal of the bottom detection circuit or the peak detection circuit, and wherein the negative phase output of the amplifier is fed back to the positive phase input of the amplifier through a feedback resistor, and the positive phase output of the amplifier is fed back to the negative phase input of the amplifier through a peak detection circuit and a feedback resistor.

According to a tenth aspect of the invention, there is provided a burst signal detection circuit, wherein the DC variation removing signal amplifier includes a master-slave type automatic threshold control circuit configured with a master bottom detection circuit or a master peak detection circuit for detecting the absolute minimum level or the absolute maximum level, respectively, of the input signal, a slave peak detection circuit or a slave bottom detection circuit for detecting the relative

maximum level or the relative minimum level, respectively, of the input signal from the output signal of the master bottom detection circuit or the master peak detection circuit, and a voltage dividing circuit for  
5 generating a threshold level by dividing the output signal of the master bottom detection circuit or the master peak detection circuit and the output signal of the slave peak detection circuit or the slave bottom detection circuit.

10 According to an 11th aspect of the invention, there is provided a burst signal detection circuit, wherein the DC variation removing signal amplifier includes a master-slave type automatic threshold control circuit configured with a master bottom detection circuit or a master peak  
15 detection circuit for detecting the absolute minimum level or the absolute maximum level, respectively, of the input signal, a voltage dividing circuit for generating a voltage divided signal by dividing the voltage of the output signal and the input signal of the master bottom  
20 detection circuit or the master peak detection circuit, and a slave peak detection circuit or a slave bottom detection circuit for generating a threshold level by detecting the relative maximum level or the relative minimum level, respectively, of the voltage divided  
25 signal from the output signal of the master bottom detection circuit or the master peak detection circuit.

According to a 12th aspect of the invention, there is provided a burst signal detection circuit, wherein the master-slave type automatic threshold control circuit  
30 connects the level hold capacitor of the slave peak detection circuit or the slave bottom detection circuit to the output of the master bottom detection circuit or the master peak detection circuit.

According to a 13th aspect of the invention, there  
35 is provided a burst signal detection circuit, wherein the amplitude identifying circuit includes a peak detection circuit or a bottom detection circuit for detecting the

maximum level or the minimum level, respectively, of the input signal, an threshold level control circuit for generating an threshold level, and a comparator circuit for comparing the output level of the peak detection circuit or the bottom detection circuit with the threshold level.

According to a 14th aspect of the invention, there is provided a burst signal detection circuit, wherein the amplitude identifying circuit includes a peak detection circuit and a bottom detection circuit for detecting the maximum level and the minimum level, respectively, of the input signal, a threshold level control circuit for generating an threshold level by shifting the output level of the bottom detection circuit or the peak detection circuit by a predetermined amount, and a comparator circuit for comparing the output level of the peak detection circuit or the bottom detection circuit with the threshold level.

According to a 15th aspect of the invention, there is provided a burst signal detection circuit wherein the amplitude identifying circuit includes a peak detection circuit and a bottom detection circuit for detecting the maximum level and the minimum level, respectively, of the input signal, a threshold level control circuit for producing a first threshold level by shifting the output level of the bottom detection circuit by a predetermined amount and producing a second threshold level by shifting the output level of the peak detection circuit by a predetermined amount, and a comparator circuit for comparing the first threshold level and the second threshold level with each other.

According to a 16th aspect of the invention, there is provided a burst signal detection circuit, wherein the threshold level control circuit includes a temperature compensating circuit for changing the threshold level with a temperature change to thereby compensate for the variation of the gain due to the temperature change.

According to a 17th aspect of the invention, there is provided a burst signal detection circuit, wherein the threshold level control circuit includes a reference voltage circuit for changing the threshold level with the change in the source voltage thereby to compensate for the variation of the gain due to the change in the source voltage.

According to an 18th aspect of the invention, there is provided a burst signal detection circuit, further comprising a photo diode for receiving the optical signal and a preamplifier for converting the current signal output by the photo diode into a voltage signal, wherein the arrival of the burst signal is detected from the output signal of the preamplifier.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing a configuration according to a first embodiment of the invention;

Figs. 2A - 2C are diagrams showing operating waveforms according to the first embodiment of the invention;

Figs. 3A and 3B are diagrams showing a configuration of the bottom detection circuit and the threshold level control circuit according to the first embodiment of the invention;

Fig. 4 is a diagram showing a configuration according to a second embodiment of the invention;

Fig. 5 is a diagram showing a configuration according to a third embodiment of the invention;

Figs. 6A - 6C are diagrams showing operating waveforms according to the third embodiment of the invention;

Fig. 7 is a diagram showing a configuration of the threshold level control circuit according to the third embodiment of the invention;

Fig. 8 is a diagram showing a configuration according to a fourth embodiment of the invention;

Figs. 9A - 9C are diagrams showing operating

waveforms according to the fourth embodiment of the invention;

5 Figs. 10A and 10B are diagrams showing a configuration of the threshold level control circuit according to the fourth embodiment of the invention;

Fig. 11 is a diagram showing a configuration according to a fifth embodiment of the invention;

10 Figs. 12A -12C are diagrams showing operating waveforms according to the fifth embodiment of the invention;

Fig. 13 is a diagram showing a configuration of the master-slave type automatic threshold control (ATC) circuit according to the fifth embodiment of the invention;

15 Fig. 14 is a diagram showing a configuration of the threshold level control circuit according to the fifth embodiment of the invention;

Fig. 15 is a diagram showing a configuration according to a sixth embodiment of the invention;

20 Figs. 16A - 16C are diagrams showing operating waveforms according to the sixth embodiment of the invention;

25 Fig. 17 is a diagram showing a configuration of the master-slave type automatic threshold control (ATC) circuit according to the sixth embodiment of the invention;

Fig. 18 is a diagram showing a configuration of the threshold level control circuit according to the sixth embodiment of the invention;

30 Fig. 19 is a diagram showing a configuration according to a seventh embodiment of the invention;

Figs. 20A and 20B are diagrams showing operating waveforms according to the seventh embodiment of the invention;

35 Fig. 21 is a diagram for explaining the conventional burst signal detection circuit;

Figs. 22A and 22B are diagrams showing operating

waveforms for the conventional burst signal detection circuit; and

Figs. 23A - 23C are diagrams for explaining the frequency response of a light-receiving element and the DC level variation of the burst signal.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a configuration of a first embodiment of the invention. Figs. 2A to 2C show operating waveforms of the same embodiment. In Fig. 1, a burst signal detection circuit for an optical burst signal receiver is shown. In the figure, reference numeral 10 designates a photo-diode (PD), numeral 11 a preamplifier, numeral 12 a DC variation removing circuit, numeral 13 a signal amplifier, numeral 14 an automatic threshold control (ATC) circuit, numeral 15 an amplitude identifying circuit, numeral 16 an amplitude detection circuit and numeral 17 a identifying circuit.

The photo-diode (PD) 10 converts the arriving optical signal into a current signal, and the preamplifier 11 converts the current signal output from the photo-diode (PD) 10 into a voltage signal by means of an amplifier 11A, a resistor 11B and an inverting buffer amplifier 11C.

The DC variation removing circuit 12 applies the output signal of the preamplifier 11 to the bottom detection circuit 12A and the differential amplifier 12B. The bottom detection circuit 12A detects and outputs the bottom level of the output signal of the preamplifier 11 including the DC level variation, and differentially amplifies the output signal of the preamplifier 11 and the bottom level by means of the differential amplifier 12B. Thus, a signal is output in which the DC level variation is removed.

The differential amplifier 12B is set to have a low gain in order to reduce the waveform distortion due to the output saturation and thus operates as a buffer. The differential amplifier 12B can of course be designed with

any gain to operate other than as a buffer.

The signal amplifier 13 amplifies the weak signal output from the preamplifier 11 to thereby produce a sufficiently large logic signal. The signal amplifier 13 includes an automatic threshold control (ATC) circuit 14 and a limiter amplifier 13A to meet the requirement of the burst-like signal.

The automatic threshold control (ATC) circuit 14 includes a peak detection circuit 14A, a bottom detection circuit 14B and a voltage dividing circuit 14C. Upon application of a burst signal thereto, the peak detection circuit 14A and the bottom detection circuit 14B instantaneously detect and output a maximum value and a minimum value, respectively of the input signal. The voltage dividing circuit 14C, on the other hand, divides the voltage of the maxim and minimum levels output from the peak detection circuit 14A and the bottom detection circuit 14B by a resistor, and sets the threshold level to the central level of the input signal.

The signal amplifier 13 applies the threshold level set by the voltage dividing circuit 14C and the input signal from the DC variation removing circuit 12 to the limiter amplifier 13A and, even when the burst signals have small levels, amplifies and outputs the received signal at a predetermined amplitude level.

The amplitude identifying circuit 15 is supplied with the signal from which the DC level variation is removed by the DC variation removing circuit 12, and the peak level thereof is detected by the peak detection circuit 16A of the amplitude detection circuit 16. The particular peak level and the threshold level output from the threshold level control circuit 17A of the identifying circuit 17 are applied to a comparator 15A. The comparator 15A outputs a detection signal indicating the presence or absence of a burst signal in accordance with whether the peak level has exceeded the threshold level or not.

Figs. 2A to 2C show an example of the operating waveforms according to the embodiment shown in Fig. 1, wherein Fig. 2A shows a waveform in the DC variation removing circuit 12; Fig. 2B shows a waveform in each circuit in the amplitude identifying circuit 15, and Fig. 2C shows a waveform of the output from the comparator 15A in the amplitude identifying circuit 15.

The examples of the operating waveforms shown in Figs. 2A to 2C represent the waveforms of a burst signal (packet #2), similar to that shown in Fig. 23, having a small amplitude arriving immediately after a burst signal (packet #1) of a large amplitude. The DC variation removing circuit 12 is supplied with an output signal (a) indicated by solid line in Fig. 2A from the preamplifier 11, and the bottom detection circuit 12A of the DC variation removing circuit 12 outputs the bottom level (b) indicated by the dotted line in Fig. 2A.

The amplitude identifying circuit 15 is supplied with a signal (c) indicated by the dotted line in Fig. 2B from the DC variation removing circuit 12, and the peak detection circuit 16A in the amplitude identifying circuit 15 outputs a detected peak level (d) indicated by solid line in Fig. 2B.

The detected peak level output from the peak detection circuit 16A is reset within a guard time. The reset signal (g) in Fig. 2B is generated at a predetermined timing within the guard time, and the peak detection level is reset by this reset signal (g). This is also the case with the peak detection circuit 14A and the bottom detection circuits 12A and 14B in the other circuits.

When the detected peak level (d) exceeds the threshold level (e) (Fig. 2B), the comparator 15A in the amplitude identifying circuit 15 outputs a detection signal (f) indicating the presence of a burst signal as shown in Fig. 2C.

As described above, according to the invention,



before detecting the amplitude by the amplitude identifying circuit 15, the DC level variation is removed by the DC variation removing circuit 12. Therefore, the burst signal can be accurately detected regardless of the variation of the DC level due to the low frequency response of the photo-diode (PD), etc.

The bottom detection circuit 12A in the DC variation removing circuit 12, as shown in Fig. 3A, for example, can be configured with an amplifier 12A<sub>1</sub>, a diode 12A<sub>2</sub>, a capacitor 12A<sub>3</sub>, and a buffer amplifier 12A<sub>4</sub>.

The threshold level control circuit 17A, on the other hand, can be configured, as shown in Fig. 3B for example, with a reference voltage source (BGR: band gap reference) 17A<sub>1</sub>, an operational amplifier 17A<sub>2</sub>, and resistors 17A<sub>3</sub> and 17A<sub>4</sub>.

Assume that the reference voltage output from the reference voltage source (BGR) 17A<sub>1</sub> is V<sub>0</sub> and the resistance values of the resistors 17A<sub>3</sub> and 17A<sub>4</sub> are R<sub>I0</sub> and R<sub>I1</sub>. The threshold level V<sub>REF</sub> output from the threshold level control circuit 17A is given by equation (1) below.

$$V_{REF} = \{R_{I1}/(R_{I0} + R_{I1})\} * V_0 \quad (1)$$

By changing the voltage dividing ratio of the resistance values R<sub>I0</sub> and R<sub>I1</sub>, the threshold level can be adjusted.

The threshold level control circuit 17A can of course assume various configurations other than the example configuration shown in Fig. 3B. In the embodiments described below also, the invention can assume various configurations modified based on the modification of the basic configuration thereof.

Fig. 4 is a diagram showing a configuration according to a second embodiment of the invention. According to the second embodiment, in place of the preamplifier 11 in the first embodiment described above, a preamplifier 41 is configured with one amplifier 41A and a resistor 41B. As a result, the signal output from

the preamplifier 41 is inverted in polarity as compared with the first embodiment.

Thus, according to the second embodiment, the bottom detection circuit 12A of the DC variation removing circuit 12 in the first embodiment is replaced with a peak detection circuit 42A to detect the DC level variation.

Specifically, in the DC variation removing circuit 42, the differential amplifier 12B differentially amplifies the output signal of the peak detection circuit 42A for detecting the DC level variation and the output signal of the preamplifier 41 thereby to remove the DC level variation component from the output signal of the preamplifier 41.

The other parts of the configuration remain the same as the first embodiment, and like in the first embodiment, the presence or absence of a burst signal can be accurately detected from the signal of which the DC variation is removed. In Fig. 4, the same component elements as the corresponding ones in the first embodiment are designated by the same reference numerals, respectively and will not be described again.

In the other embodiments described below also, as in the first embodiment described above, components with an inverted input signal polarity can make up a configuration with inverted logic. The operating principle, however, remains similar and will not be explained again.

Fig. 5 shows a configuration of the third embodiment of the invention, and Fig. 6 shows operating waveforms thereof. In Fig. 5, like Fig. 1, a burst signal detection circuit of an optical burst signal receiver is shown. In this third embodiment, a level shift circuit 52C is added to the output of the bottom detection circuit 12A for detecting the DC level variation in the DC variation removing circuit 52.

If the level shift circuit 52C is not provided, the

output of the differential amplifier 12B can assume only positive values, and therefore only one half region of the linear output range can be used so that the output level of the differential amplifier 12B is liable to be saturated and the waveform is liable to be distorted.

In contrast, by adding the level shift circuit 52C, the negative linear output range can also be used for the output of the differential amplifier 12B. Thus, the saturation of the output level can be prevented and the waveform distortion can be reduced.

Also, according to the third embodiment, the amplitude detection circuit 56 in the amplitude identifying circuit 55 includes the peak detection circuit 16A and a bottom detection circuit 56B for detecting both a peak level and a bottom level.

By means of the threshold level control circuit 57A providing a predetermined current and a resistor 57B, the threshold level in the amplitude identifying circuit 55 is generated by shifting a predetermined voltage from the bottom level detected by the bottom detection circuit 56B in the amplitude detection circuit 56.

In the first embodiment described above, since the amplitude detection circuit 16 detects the level of only one side (peak side), the output level is affected by the DC operating point of the differential amplifier 12B. In the third embodiment, in contrast, since the threshold level is generated by shifting to the bottom level, the amplitude component alone can be detected without being affected by the DC operating point.

Figs. 6A to 6C show an example of the operating waveforms according to the third embodiment in which Fig. 6A shows a waveform of the output signal from the DC variation removing circuit 52; Fig. 6B shows a waveform in each circuit in the amplitude identifying circuit 55; and Fig. 6C shows a waveform of the comparator 15A in the amplitude identifying circuit 55.

The DC variation removing circuit 52 is supplied

with a signal (a) indicated by solid line in Fig. 6A from the preamplifier 11. The bottom level detected by the bottom detection circuit 12A in the DC variation removing circuit 52 is shifted to the level (b) indicated by a dotted line in the vicinity of the center of the output signal level of the preamplifier 11 and is input to the differential amplifier 12B. Thus, the differential amplifier 12B outputs a signal assuming both negative and positive values with respect to a level to which the bottom level is shifted by a predetermined amount.

The amplitude identifying circuit 55, on the other hand, is supplied with a signal (c) indicated by a dotted line in Fig. 6B from the DC variation removing circuit 52, and the peak detection circuit 16A in the amplitude identifying circuit 55 outputs a detected peak level (d) indicated by a solid line in Fig. 6B.

The bottom detection circuit 56B in the amplitude identifying circuit 55 outputs a detected bottom level (e) indicated by a solid line in Fig. 6B. The bottom level is shifted by a predetermined amount by the threshold level control circuit 57A and the resistor 57B to a threshold level (f) indicated by a solid line in Fig. 6B. The threshold level (f) is input to the comparator 15A.

When the peak level (d) output from the peak detection circuit 16A in the amplitude detection circuit 56 exceeds the threshold level (f) (Fig. 6B), the comparator 15A outputs a detection signal (g) indicating the presence of the burst signal as shown in Fig. 6C.

Fig. 7 shows an example configuration of the threshold level control circuit 57A according to the third embodiment of the invention. The threshold level control circuit 57A includes a reference voltage circuit 71, a current regulating circuit 72 and a current mirror circuit 73.

The reference voltage circuit 71 includes a reference voltage source (BGR) 71A, and a voltage

dividing circuit 71B having resistors  $R_{R1}$  and  $R_{R2}$  of resistance values  $R_{R1}$  and  $R_{R2}$ . The current regulating circuit 72 includes an operational amplifier 72A, an NMOS transistor 72B, a variable resistor 72C of resistance value  $R_{10}$ , and a thermistor 72D of a resistance value  $R_{11}$ . The current mirror circuit 73 includes two PMOS transistors 73A and 73B.

The threshold level control circuit 57A outputs a reference current  $I_0$  from the current mirror circuit 73 based on the reference voltage output  $V_0$  from the reference voltage circuit 71, and shifts the detected bottom level by the voltage drop  $\Delta V_{REF}$  due to the reference current  $I_0$  and the reference resistor 57B in the threshold level control circuit 57 shown in Fig. 5 to generated the threshold level  $V_{REF}$ .

Let  $V_{BT}$  be the detected bottom level output from the bottom detection circuit 56B in the amplitude detection circuit in Fig. 5,  $R_{REF}$  be the resistance value of the reference resistor 57B,  $V_1$  be the output voltage of the reference voltage source (BGR) 71A in the reference voltage circuit 71 in Fig. 7, and  $V_{DD}$  a supply voltage. The threshold level output  $V_{REF}$  from the threshold level control circuit 57 is expressed by equation (2) below.

$$\begin{aligned} V_{REF} &= V_{BT} + I_0 * R_{REF} = V_{BT} + (V_0 / (R_{10} + R_{11})) * R_{REF} \\ &= V_{BT} + \{ (R_{R1} * V_1 + R_{R2} * V_{DD}) / (R_{R1} + R_{R2}) \} * \\ &\quad \{ R_{REF} / (R_{10} + R_{11}) \} \end{aligned} \quad (2)$$

The variable resistor 72C and the thermistor 72D of the resistance values  $R_{10}$  and  $R_{11}$ , respectively, are resistors connected outside of the LSI. The variable resistor 72C is for current regulation and the thermistor 72D is a resistor for temperature compensation. In the case where the thermistor 72D (resistance value  $R_{11}$ ) has a positive temperature coefficient, the temperature coefficient of the threshold level is negative.

In this configuration example of the threshold level control circuit, the threshold level is compensated for the gain variation of the preamplifier 11 or the DC

variation removing circuit 52 in accordance with the variation in power supply. As a result, the threshold level irregularity due to the gain variation for detecting the presence or absence of the burst signal can be reduced.

Fig. 8 shows a configuration of a fourth embodiment of the invention, and Fig. 9 shows operating waveforms thereof. In the fourth embodiment, instead of providing the DC variation removing circuit as an independent circuit, the function of removing the DC variation is built in a signal amplifier 83, and the output of the DC variation removing signal amplifier is input to an amplitude identifying circuit 85 to thereby simplify the circuit elements.

The DC variation removing signal amplifier 83 includes a bottom detection circuit 83A, an amplifier 84 and a limiter amplifier 83B. The amplifier 84 includes an amplifier 84A, a peak detection circuit 84B and resistors 84C, 84D, 84E, and 84F.

The amplitude identifying circuit 85 includes an amplitude detection circuit 86, a identifying circuit 87 and a comparator 85A. The amplitude detection circuit 86 includes a peak detection circuit 86A and a bottom detection circuit 86B. The identifying circuit 87 includes a threshold level control circuit 87A and resistors 87B, 87C.

Figs. 9A to 9C show operating waveforms according to the fourth embodiment. Fig. 9A shows a waveform of the output signal from the DC variation removing signal amplifier 83, Fig. 9B a waveform in each circuit of the amplitude identifying circuit 85, and Fig. 9C a waveform of the comparator 85A in the amplitude identifying circuit 85.

To the DC variation removing signal amplifier 83, a signal (a) indicated by a dotted line in Fig. 9A is input, and the bottom detection circuit 83A in the DC variation removing signal amplifier 83 outputs a detected

bottom level (b) indicated by a solid line in Fig. 9C.

The detected bottom level (c) is input to one input terminal of the amplifier 84A through a resistor 84D. To the input terminal, the peak level detected by the peak detection circuit 84B from the positive phase output of the amplifier 84A is also input. As a result, a level in the vicinity of the central portion of the received signal level is determined as a threshold level.

To the other input terminal of the amplifier 84A, the output signal from the preamplifier 11 and the negative phase output of the amplifier 84A through the resistors 84C and 84E are input. Thus, the amplifier 84A can output a voltage with either a positive or negative value with respect to the vicinity of the central portion of the received signal level, thereby outputting an amplified signal in which the DC variation has been removed.

The output signal of the DC variation removing signal amplifier 83 is input to the amplitude identifying circuit 85. This signal is indicated by a dotted line (c) in Fig. 9B. In the signal amplitude identifying circuit 85, the peak detection circuit 86A detects and outputs the peak level (d) of the input signal (c). The detected peak output (d) is input to one input terminal of the comparator 85B through the resistor 87B.

The bottom detection circuit 86B in the amplitude identifying circuit 85 detects and outputs the bottom level (e) of the input signal (c), and the detected bottom output (e) is input to the other input terminal of the comparator 85A through the resistor 87C.

Further, to the input terminals of the comparator 85A, a level shifting current is input from the threshold level control circuit 87A. The detected peak output (d) described above is shifted to an amplitude threshold level #1 indicated by (f) in Fig. 9B, while the detected bottom output (e) is shifted to an amplitude threshold level #2 indicated by (g) in Fig. 9B. When the amplitude

threshold level #1 indicated by (f) exceeds the amplitude threshold level #2 of (g), the comparator 85A outputs the detection signal (h) indicating the presence of a burst signal as shown in Fig. 9C.

5       According to the fourth embodiment, a weak signal is amplified by the DC variation removing signal amplifier 83, and the amplitude thus increased is detected for amplitude identification. Thus, the presence or absence of the burst signal can be detected more accurately.

10       In this embodiment, the DC variation removing signal amplifier 83 constitutes an automatic threshold control (ATC) circuit of feedback type for feeding back the positive phase output of the amplifier 84A to the input side through the peak detection circuit 84B and the  
15       resistor 84F. At the same time, the negative phase output of the amplifier 84A is fed back to the input side through the resistor 84E. The amplifier inserted before the amplitude identifying circuit and having the function of removing the DC variation, however, is not necessarily  
20       limited to the above-mentioned amplifier but can be variously modified.

      Fig. 10A shows an example configuration of the threshold level control circuit 87A according to the fourth embodiment of the invention. As shown in Fig.  
25       10A, the threshold level control circuit 87A includes a reference voltage circuit 10A, a current regulating circuit 102 and a current output circuit 103. The threshold level control circuit 87A is similar to the threshold level control circuit 57A in the third  
30       embodiment in that the gain variation is compensated by the threshold level.

      The reference voltage circuit 101 includes a reference voltage source (BGR) 101A and a voltage dividing circuit including resistors with resistance  
35       values  $R_{R1}$  and  $R_{R2}$ . The voltage regulating circuit 102 includes an operational amplifier 102A, a variable resistor 102B with a resistance value  $R_{T0}$  and a



thermistor 102C with a resistance value  $R_{11}$ . The current output circuit 103, on the other hand, includes a buffer amplifier 103A for outputting an amplitude identifying signal #2, a resistor 103C with a resistance value  $R_{OUT}$ , a  
 5 buffer amplifier 103B for outputting an amplitude identifying signal #1 of lower level than the amplitude identifying signal #2, and a resistor 103D with a resistance value  $R_{OUT}$ .

The amplitude identifying signal #2 and the  
 10 amplitude identifying signal #1 output from the threshold level control circuit 87A are input to the comparator 85A in Fig. 8 together with the output of the peak detection circuit 86A and the bottom detection circuit 86B.

Thus, the comparator 85A is supplied with the peak  
 15 level  $V_{PK}$  detected by the peak detection circuit 86A, the bottom level  $V_{BT}$  detected by the bottom detection circuit 86B, and the amplitude level #1 ( $V_{REF1}$ ) of the signal (f) and the amplitude level #2 ( $V_{REF2}$ ) of the signal (g) obtained by dividing the output voltages  $V_3$  and  $V_4$  of the  
 20 buffer amplifiers 103A and 103B connected to the output of the threshold level control circuit 87A shown in Fig. 10A. The input levels are compared with each other by the comparator 85A.

The amplitude levels  $V_{REF1}$  and  $V_{REF2}$  and the difference  
 25 thereof  $V_{REF1} - V_{REF2}$  are expressed by the equations below.

$$\begin{aligned} V_{REF1} &= (R_{OUT} * V_{PK} + R_{REF} * V_3) / (R_{OUT} + R_{REF}) \\ &= R_{OUT} * V_{PK} / (R_{OUT} + R_{REF}) + \{R_{REF} / (R_{OUT} + R_{REF})\} * \\ &\quad \{(R_{R1} * V_1 + R_{R2} * V_{DD}) / (R_{R1} + R_{R2})\} \end{aligned} \quad (3-1)$$

$$\begin{aligned} V_{REF2} &= (R_{OUT} * V_{BT} + R_{REF} * V_4) / (R_{OUT} + R_{REF}) \\ 30 \quad &= R_{OUT} * V_{BT} / (R_{OUT} + R_{REF}) + \{R_{REF} / (R_{OUT} + R_{REF})\} * \\ &\quad \{R_{11} / (R_{10} + R_{11})\} * \{(R_{R1} * V_1 + R_{R2} * \\ &\quad V_{DD}) / (R_{R1} + R_{R2})\} \end{aligned} \quad (3-2)$$

$$\begin{aligned} V_{REF1} - V_{REF2} &= \{R_{OUT} / (R_{OUT} + R_{REF})\} * (V_{PK} - V_{BT}) - \\ &\quad \{R_{REF} / (R_{OUT} + R_{REF})\} * \{R_{10} / (R_{10} + R_{11})\} * \\ 35 \quad &\{(R_{R1} * V_1 + R_{R2} * V_{DD}) / (R_{R1} + R_{R2})\} = \\ &\quad \{R_{OUT} / (R_{OUT} + R_{REF})\} * (V_{PK} - V_{BT}) - \Delta V_{REF} \end{aligned} \quad (3-3)$$

In the threshold level control circuit according to

the third embodiment shown in Fig. 7, as seen from equation (2), is such that the threshold level  $V_{REF}$  depends on the ratio between the resistors  $R_{10}$  and  $R_{11}$  which are provided in an external area of the LSI and the internal resistor  $R_{REF}$  of the LSI. This resistance changes with the temperature difference between the interior and exterior, thereby changing the threshold level according to the temperature of the operating environment. In the case where the threshold level control circuit shown in Figs. 10A, 10B is used, on the other hand, the voltage input to the comparator, as seen from equation (3-3), constitutes the term of the resistance ratio between the internal resistors or between the external resistors. Thus, a high-accuracy threshold level control, which is stable against the temperature difference between the exterior and interior or the change thereof, is possible.

In place of the voltage regulating circuit 102, as shown in Fig. 10B, a voltage regulating circuit 102' including an operational amplifier 102A, a variable resistor 102D and two thermistors 102E and 102F can be used. In such a case, both the amplitude identifying signal #1 and the amplitude identifying signal #2 can be temperature-compensated thereby to make possible a more accurate temperature compensation.

Fig. 11 shows a configuration according to a fifth embodiment of the present invention. Fig. 12 shows operating waveforms of this embodiment. In the fifth embodiment, a master-slave type automatic threshold control (ATC) circuit is used as a DC variation removing circuit. The other parts of the configuration are similar to those of the third embodiment shown in Fig. 5, and will not be described again.

In the aforementioned DC variation removing circuit using the bottom detection circuit and the differential amplifier, the DC variation detection signal output from the bottom detection circuit is not at the central level

of the input signal. In the case where the gain of the differential amplifier is increased, therefore, the problem is posed that the high-level ("1") side of the output signal is saturated, thereby deteriorating the pulse width.

The master-slave type automatic threshold control (ATC) circuit 112 in the DC variation removing signal amplifier 111 according to the embodiment shown in Fig. 11, on the other hand, includes a peak detection circuit 112A, a bottom detection circuit 112B and a voltage dividing circuit 112C, and the peak detection circuit 112A is configured to detect the relative maximum level from the bottom detection level and output a detected peak level.

Also, the central level between the bottom detection level and the detected peak level, determined by the voltage dividing circuit 112C, is set as a threshold signal of the differential amplifier 12B. Therefore, while the threshold signal follows the DC variation, it can be set at the central level of the input signal, thereby preventing the deterioration of the pulse width even with an increased gain of the differential amplifier 12B.

Figs. 12A to 12C show an example of operating waveforms, according to the fifth embodiment shown in Fig. 11, in which Fig. 12A shows waveforms in the DC variation removing signal amplifier 111, Fig. 12B shows waveforms in the peak detection circuit 16A, the bottom detection circuit 56B and the threshold level control circuit 57A in the amplitude identifying circuit 55, and Fig. 12C shows a waveform of the output signal from the comparator 15A in the amplitude identifying circuit 55.

To the DC variation removing signal amplifier 111, a signal (a) indicated by a dotted line in Fig. 12A is supplied from the preamplifier 11. The bottom detection circuit 112B in the DC variation removing signal amplifier 111 detects and outputs the bottom level (c).

The peak detection circuit 112A detects and outputs the relative peak level (b) from the bottom level (c), and the voltage dividing circuit 112C outputs the peak level (b) and the central level (d) of the bottom level (c) as an output signal of the automatic threshold control (ATC) circuit 112.

Also, to the amplitude identifying circuit 55, the signal (e) indicated by a dotted line in Fig. 12B is supplied from the DC variation removing signal amplifier 111. The peak detection circuit 16A in the amplitude identifying circuit 55 outputs the detected peak level (f) shown in Fig. 12B.

The bottom detection circuit 56B in the amplitude identifying circuit 55 outputs the detected bottom level (g) shown in Fig. 12B, and the threshold level (h) in Fig. 12B obtained by shifting the bottom level (g) by a predetermined amount by the threshold level control circuit 57A and the resistor 57B is input to the comparator 15A.

Once the peak level (f) output from the peak detection circuit 16A in the amplitude detection circuit 56 exceeds the threshold level (h), the comparator 15A outputs the detection signal (i) indicating the presence of a burst signal as shown in Fig. 2C.

Fig. 13 shows an example configuration of the master-slave automatic threshold control (ATC) circuit according to the fifth embodiment of the invention. The master bottom detection circuit 112B includes an amplifier 132A, a buffer amplifier 132B, a diode 132C and a capacitor 132D for detecting the absolute minimum level.

The slave peak detection circuit 112A includes an amplifier 131A, a buffer amplifier 131B, a diode 131C and a capacitor 131D. Also, the output of the master bottom detection circuit 112B is connected to an end of the capacitor 131D thereby to detect the relative maximum level from the detected bottom level.

According to the fifth embodiment, the DC level variation due to the low frequency response of the photo-diode (PD) is first detected by the master bottom detection circuit 112B, and the output of the slave peak detection circuit 12A is followed by the detected bottom level, and these signals are divided by the voltage dividing circuit 112C. While the threshold level generated in the automatic threshold control (ATC) circuit follows the DC level variation, it can be set to the center of the amplitude of the input signal.

Fig. 14 shows an example configuration of the threshold level control circuit according to the fifth embodiment. This threshold level control circuit includes a reference voltage circuit 141 having a temperature reference voltage circuit 144, a reference voltage source (BGR) 141A, an amplifier 145 and a voltage dividing circuit 141B, a voltage regulating circuit 142 and a current mirror circuit 143.

The threshold level control circuit is similar to the threshold level control circuit according to the third embodiment described above in that a reference current  $I_0$  is output from the current mirror circuit 143 in the last stage, and the detected bottom level is shifted to provide a threshold level.

The threshold level control circuit shown in Fig. 14 utilizes the temperature reference voltage circuit 144 with a field effect transistor (FET) in the LSI but not an external thermistor in order to give a temperature inclination of the threshold level. As a result, the external parts can be reduced and a simplified configuration is obtained.

The threshold level  $V_{REF}$  applied to the comparator 15A is expressed by equations (4-1) and (4-2) below, where the temperature inclination is given by the term of  $V_2$  in equation (4-2) and the supply voltage inclination by the term of  $V_{DD}$ .

$$\begin{aligned} V_{REF} &= V_{BT} + I_0 * R_{REF} \\ &= V_{BT} + \{V_0 / (R_{I0} + R_{I1})\} * R_{REF} \end{aligned} \quad (4-1)$$

$$\begin{aligned} V_0 &= \{R_{R4} / (R_{R3} + R_{R4})\} * (R_{R2} / R_{R1}) * V_1 - \{R_{R4} / (R_{R3} + \\ &R_{R4})\} * (R_{R2} / R_{R1}) * V_2 + \{R_{R3} / (R_{R3} + R_{R4})\} * V_{DD} \end{aligned}$$

(4-2)

where  $V_0$  is the output voltage of the reference voltage circuit 141,  $V_1$  is the output voltage of the reference voltage source (BGR) 141A,  $V_2$  is the temperature reference voltage obtained from the temperature reference voltage circuit 144 and  $V_{DD}$  is the supply voltage.

The temperature reference voltage  $V_2$  is expressed in a form inversely proportional to the gain coefficient  $\beta$  of the MOS-FET as shown in equation (5) below. The temperature coefficient of the gain coefficient  $\beta$  of the MOS-FET is negative and therefore the temperature coefficient of the value of the temperature reference voltage  $V_2$  is positive.

$$V_2 = (1/R) * (2/\beta) * \{1 - \sqrt{1/k}\} \quad (5)$$

Fig. 15 shows a configuration according to a sixth embodiment of the invention, and Fig. 16 shows the operating waveforms thereof. According to the sixth embodiment, the input signal is amplified by a differential amplifier 12B in a DC variation removing signal amplifier 151, after which the resulting signal is further amplified by an amplifier 153 and applied to an amplitude identifying circuit 155. As a result, a weak input signal is amplified and the amplitude thus increased is identified, so that the presence or absence of a burst signal can be surely detected.

Also, in the automatic threshold control (ATC) circuit 152 in the DC variation removing signal amplifier 151, the input signal level and the bottom level output from the bottom detection circuit 152B are divided by the voltage dividing circuit 152C thereby to produce a voltage divided signal, which is applied to a peak detection circuit 152A and the peak detection output

thereof is set as a threshold signal. In this way, the amplifier inserted before amplitude identification can be variously configured.

Also according to this embodiment, the output of the comparator 15A is positively fed back to the input thereof through a resistor 155A, and the output of the peak detection circuit 16A is input to the comparator 15A through a resistor 155B thereby to set a hysteresis. By thus setting a hysteresis, even in the case where the output signal of the amplitude detection circuit 56 is weak and is liable to be affected by noises, the effect of the noises can be removed and the presence or absence of the burst signal can be positively detected.

Figs. 16A to 16C show an example of the operating waveforms according to the sixth embodiment shown in Fig. 15. Fig. 16A shows a waveform of the DC variation removing signal amplifier 151, Fig. 16B waveforms of the peak detection circuit 16A, the bottom detection circuit 56B and the threshold level control circuit 57A in the amplitude identifying circuit 155, and Fig. 16C a waveform of the comparator 15A in the amplitude identifying circuit 155.

The DC variation removing signal amplifier 151 is impressed with the signal (a) indicated by dotted line in Fig. 16A from the preamplifier 11, and the bottom detection circuit 152B in the DC variation removing signal amplifier 151 detects and outputs the bottom level (c).

To the peak detection circuit 152A, the voltage divided level (b) between the bottom level (c) and the input signal (a) is supplied. The peak level is output as an output (d) of the automatic threshold control (ATC) circuit. The waveforms of Figs. 16B, 16C are similar to those of Figs. 12B, 12C and therefore will not be described again.

Fig. 17 shows an example configuration of the master-slave type automatic threshold control (ATC)

circuit according to a sixth embodiment. A master bottom detection circuit 172 detects the absolute minimum level, and a voltage dividing circuit 173 generates a voltage division level which is half way between the bottom detection level and the input signal level.

One terminal of a peak hold capacitor 171D in the slave peak detection circuit 171 is connected to the output of the master bottom detection circuit 172, and therefore the central level of amplitude is detected as a relative peak level from the detected bottom level.

Fig. 18 shows an example configuration of the threshold level control circuit according to the sixth embodiment. This configuration example includes a reference voltage circuit 181 having a temperature reference voltage circuit 186, a reference voltage source (BGR) 181A, a differential amplifier 185 and a voltage dividing circuit 181B, a voltage regulating circuit 182, a current source circuit 183 and a current mirror circuit 184. In this embodiment, a temperature reference voltage  $V_2$  is generated due to the internal FET with a configuration simple as compared with the example configuration of the threshold level control circuit according to the embodiment shown in Fig. 14.

In this configuration example of the threshold level control circuit, the threshold level  $V_{REF}$  is expressed by equation (6) below, and similar to the configuration of the threshold level control circuit according to the fourth and fifth embodiments, the threshold level is determined by voltage division between the internal resistors or between the external resistors. Thus the threshold level regulation with high accuracy is possible.

$$\begin{aligned} V_{REF} &= V_{BT} + I_0 * R_{REF} \\ &= V_{BT} + \{R_{I1}/(R_{I0} + R_{I1})\} * (V_0/R_{I3}) * R_{REF} \end{aligned} \quad (6)$$

The temperature reference voltage  $V_2$ , as shown in equation (7) below, is expressed in a form inversely proportional to the square root of the gain coefficient  $\beta$



of the MOS.

$$V_z = \{1 - \sqrt{1/k}\} * \sqrt{2 * I_D/\beta} \quad (7)$$

Fig. 19 shows a configuration according to a seventh embodiment of the invention, and Fig. 20 the operating waveforms thereof. According to the seventh embodiment, a peak detection circuit 196A and a bottom detection circuit 196B of master-slave type are used as an amplitude detection circuit 196 in an amplitude identifying circuit 195, and the DC level variation is removed by the amplitude detection circuit 196.

The master-slave type peak detection circuit 196A and the bottom detection circuit 196B can be configured the same way as the circuits shown in Figs. 13 and 17. Also, this configuration is similar to the configuration example of Fig. 11 except that the input signal of the amplitude identifying circuit 195 makes up an output signal of the preamplifier 11. Therefore, the same component elements are designated by the same reference numerals, respectively, and will not be described.

Figs. 20A and 20B show operating waveforms according to the seventh embodiment, in which Fig. 20A shows a waveform in each circuit of the amplitude identifying circuit 195 and Fig. 20B a waveform of the output signal from the comparator 15A of the output signal from the amplitude identifying circuit 195.

To the amplitude identifying circuit 195, an input signal (a) indicated by a dotted line in Fig. 20A is supplied from the preamplifier 11. The master bottom detection circuit 196B outputs the detected bottom level (c), and the peak detection circuit 196A detects and outputs the relative peak level (b) with respect to the detected bottom level (c).

The detected bottom level (c) is shifted by a predetermined amount by the threshold level control circuit 57A to the threshold level (d) which is input to the comparator 15A. The comparator 15A compares the threshold level (d) with the peak level (b), and in the

case where the peak level (b) exceeds the threshold level (d), outputs a detection signal (e) indicating the presence of a burst signal.

- 5 It will thus be understood from the foregoing description that, according to the present invention, a DC variation removing circuit is inserted before amplitude detection of the input signal, so that the amplitude is identified after removing the DC level variation. Thus, regardless of the DC level variation of  
10 the input signal, the presence or absence of a burst signal can be detected with high accuracy, and the erroneous detection of the burst signal which otherwise might be caused by the signal level variation due to the low frequency response of the photo-diode (PD) can be  
15 prevented. In this way, the presence or absence of the burst signal can be accurately detected even for a weak input signal.

CLAIMS

1. A burst signal detection circuit comprising:
  - a DC variation removing circuit for detecting the bottom level or the peak level of an input signal and removing the DC level variation of the input signal based on the bottom level or the peak level; and
  - an amplitude identifying circuit for detecting the presence or absence of a burst signal in said input signal based on the output signal from the DC variation removing circuit;
- 10       said amplitude identifying circuit including:
  - an amplitude detection circuit for detecting the maximum amplitude of the output signal of
  - 15       said DC variation removing circuit;
  - a threshold level control circuit for controlling a threshold level; and
  - a comparator circuit for comparing the output level of said amplitude detection circuit with
  - 20       said threshold level and outputting a detection signal indicating the presence or absence of the burst signal.
2. The burst signal detection circuit according to claim 1, wherein said DC variation removing circuit includes a bottom detection circuit or a peak detection
- 25       circuit for detecting the bottom level or the peak level, respectively, of the input signal, and a differential amplifier for differentially amplifying the difference between the input signal and the output signal from said bottom detection circuit or said peak detection circuit.
- 30       3. The burst signal detection circuit according to claim 1, wherein said DC variation removing circuit includes:
  - a bottom detection circuit or a peak
  - 35       detection circuit for detecting the bottom level or the peak level, respectively, of the input signal;
  - a level shift circuit for shifting the output signal of said bottom detection circuit or said

peak detection circuit by a predetermined value; and  
a differential amplifier for amplifying  
the difference between the output signal of said level  
shift circuit and the input signal.

- 5        4. The burst signal detection circuit according to  
claim 1, wherein said amplitude identifying circuit  
includes:

10                a peak detection circuit or a bottom  
detection circuit for detecting the maximum level or the  
minimum level, respectively, of the output signal from  
the DC variation removing circuit;

              a threshold level control circuit for  
generating a threshold level; and

15                a comparator circuit for comparing the  
output level of said peak detection circuit or said  
bottom detection circuit with said threshold level.

20        5. The burst signal detection circuit according to  
claim 1, wherein said amplitude identifying circuit  
includes a peak detection circuit or a bottom detection  
circuit for detecting the maximum level or the minimum  
level, respectively, of the output signal from the DC  
variation removing circuit, a threshold level control  
circuit for generating a threshold level by shifting the  
output level of said bottom detection circuit or said  
25        peak detection circuit by a predetermined value; and  
              a comparator circuit for comparing the  
output level of said peak detection circuit or said  
bottom detection circuit with said threshold level.

30        6. The burst signal detection circuit according to  
claim 1, wherein said amplitude identifying circuit  
includes:

35                a peak detection circuit and a bottom  
detection circuit for detecting the maximum level and the  
minimum level, respectively, of the output signal from  
the DC variation removing circuit, a threshold level  
control circuit for generating a first threshold level by  
shifting the output level of said bottom detection

circuit by a predetermined value and generating a second threshold level by shifting the output level of said peak detection circuit by a predetermined value; and

5 a comparator circuit for comparing said first threshold level and said second threshold level with each other.

7. The burst signal detection circuit according to claim 1, wherein said threshold level control circuit includes a temperature compensating circuit for changing  
10 said threshold level in accordance with the temperature change, said temperature compensating circuit being so configured as to compensate for the variation of the gain due to the temperature change.

8. The burst signal detection circuit according to claim 1, wherein said threshold level control circuit  
15 includes a reference voltage circuit for changing said threshold level with the source voltage change, said reference voltage circuit being so configured as to compensate for the variation of the gain due to the supply voltage change.  
20

9. The burst signal detection circuit according to claim 1, further comprising a photo-diode for receiving an optical signal and a preamplifier for converting the current signal from said photo-diode into a voltage  
25 signal, wherein the arrival of a burst signal is detected from the output signal of said preamplifier.

10. A burst signal detection circuit comprising:  
a DC variation removing circuit for  
detecting the bottom level or the peak level of an input  
30 signal and removing the DC level variation of the input signal based on the bottom level or the peak level;  
a signal amplifier for amplifying the output signal of said DC variation removing circuit; and  
an amplitude identifying circuit for  
35 detecting the presence or absence of a burst signal in said input signal based on the output signal from said signal amplifier;

said amplitude identifying circuit  
including:

an amplitude detection circuit for  
detecting the maximum amplitude of the output signal of  
5 said signal amplifier;

a threshold level control circuit for  
controlling the threshold level, and a comparator circuit  
for comparing the output level of said amplitude  
detection circuit with said threshold level and  
10 outputting a detection signal indicating the presence or  
absence of the burst signal.

11. The burst signal detection circuit according to  
claim 10, wherein said DC variation removing circuit  
includes a bottom detection circuit or a peak detection  
15 circuit for detecting the bottom level or the peak level,  
respectively, of the input signal, and a differential  
amplifier for differentially amplifying the difference  
between the input signal and the output signal from said  
bottom detection circuit or said peak detection circuit.

12. The burst signal detection circuit according to  
claim 10, wherein said DC variation removing circuit  
20 includes:

a bottom detection circuit or a peak  
detection circuit for detecting the bottom level or the  
25 peak level, respectively, of the input signal;

a level shift circuit for shifting the  
output signal of said bottom detection circuit or said  
peak detection circuit by a predetermined value; and

a differential amplifier for amplifying  
30 the difference between the output signal of said level  
shift circuit and the input signal.

13. The burst signal detection circuit according to  
claim 10, wherein said amplitude identifying circuit  
includes:

a peak detection circuit or a bottom  
35 detection circuit for detecting the maximum level or the  
minimum level, respectively, of the output signal from

the DC variation removing circuit;

a threshold level control circuit for generating a threshold level; and

a comparator circuit for comparing the  
5 output level of said peak detection circuit or said  
bottom detection circuit with said threshold level.

14. The burst signal detection circuit according to  
claim 10, wherein said amplitude identifying circuit  
includes a peak detection circuit or a bottom detection  
10 circuit for detecting the maximum level or the minimum  
level, respectively, of the output signal from the DC  
variation removing circuit, a threshold level control  
circuit for generating a threshold level by shifting the  
output level of said bottom detection circuit or said  
15 peak detection circuit by a predetermined value; and

a comparator circuit for comparing the  
output level of said peak detection circuit or said  
bottom detection circuit with said threshold level.

15. The burst signal detection circuit according to  
claim 10, wherein said amplitude identifying circuit  
20 includes:

a peak detection circuit and a bottom  
detection circuit for detecting the maximum level or the  
minimum level, respectively, of the output signal from  
25 the DC variation removing circuit, a threshold level  
control circuit for generating a first threshold level by  
shifting the output level of said bottom detection  
circuit by a predetermined value and generating a second  
threshold level by shifting the output level of said peak  
30 detection circuit by a predetermined value; and

a comparator circuit for comparing said  
first threshold level and said second threshold level  
with each other.

16. The burst signal detection circuit according to  
35 claim 10, wherein said threshold level control circuit  
includes a temperature compensating circuit for changing  
said threshold level in accordance with the temperature

change, said temperature compensating circuit being so configured as to compensate for the variation of the gain due to the temperature change.

17. The burst signal detection circuit according to claim 10, wherein said threshold level control circuit includes a reference voltage circuit for changing said threshold level with the supply voltage change, said reference voltage circuit being so configured as to compensate for the variation of the gain due to the supply voltage change.

18. The burst signal detection circuit according to claim 10, further comprising a photo-diode for receiving an optical signal and a preamplifier for converting the current signal from said photo-diode into a voltage signal, wherein the arrival of a burst signal is detected from the output signal of said preamplifier.

19. A burst signal detection circuit comprising an amplitude identifying circuit including:

an amplitude detection circuit for detecting the bottom level or the peak level of an input signal, for removing the DC level variation of the input signal based on said bottom level or said peak level and for detecting the maximum amplitude of said input signal;

a threshold level control circuit for controlling a threshold level; and

a comparator circuit for comparing the output level of said amplitude detection circuit with said threshold level and outputting a detection signal indicating the presence or absence of the burst signal.

20. The burst signal detection circuit according to claim 19, wherein said amplitude detection circuit includes a master bottom detection circuit or a master peak detection circuit for detecting the absolute minimum level or the absolute maximum level, respectively, of said input signal, respectively, and a slave peak detection circuit or a slave bottom detection circuit for detecting the relative maximum level or the relative



minimum level, respectively, of said input signal from the output level of said master bottom detection circuit or said master peak detection circuit.

21. The burst signal detection circuit according to claim 20, wherein a level hold capacitor in said slave peak detection circuit or said slave bottom detection circuit of said master-slave type amplitude detection circuit is connected to the output of said master bottom detection circuit or said master peak detection circuit.

22. The burst signal detection circuit according to claim 19, wherein said amplitude identifying circuit includes:

a peak detection circuit or a bottom detection circuit for detecting the maximum level or the minimum level, respectively, of the output signal from the DC variation removing circuit;

a threshold level control circuit for generating a threshold level; and

a comparator circuit for comparing the output level of said peak detection circuit or said bottom detection circuit with said threshold level.

23. The burst signal detection circuit according to claim 19, wherein said amplitude identifying circuit includes a peak detection circuit or a bottom detection circuit for detecting the maximum level or the minimum level, respectively, of the output signal from the DC variation removing circuit, a threshold level control circuit for generating a threshold level by shifting the output level of said bottom detection circuit or said peak detection circuit by a predetermined value; and

a comparator circuit for comparing the output level of said peak detection circuit or said bottom detection circuit with said threshold level.

24. The burst signal detection circuit according to claim 19, wherein said amplitude identifying circuit includes:

a peak detection circuit and a bottom

detection circuit for detecting the maximum level and the minimum level, respectively, of the output signal from the DC variation removing circuit, a threshold level control circuit for generating a first threshold level by shifting the output level of said bottom detection circuit by a predetermined value and generating a second threshold level by shifting the output level of said peak detection circuit by a predetermined value; and

a comparator circuit for comparing said first threshold level and said second threshold level with each other.

25. The burst signal detection circuit according to claim 19, wherein said threshold level control circuit includes a temperature compensating circuit for changing said threshold level in accordance with the temperature change, said temperature compensating circuit being so configured as to compensate for the variation of the gain due to the temperature change.

26. The burst signal detection circuit according to claim 19, wherein said threshold level control circuit includes a reference voltage circuit for changing said threshold level with the supply voltage change, said reference voltage circuit being so configured as to compensate for the variation of the gain due to the supply voltage change.

27. The burst signal detection circuit according to claim 19, further comprising a photo-diode for receiving an optical signal and a preamplifier for converting the current signal from said photo-diode into a voltage signal, wherein the arrival of a burst signal is detected from the output signal of said preamplifier.

28. A burst signal detection circuit comprising:  
a DC variation removing signal amplifier for detecting the bottom level or the peak level of an input signal, for removing the DC level variation of the input signal based on the bottom level or the peak level, and for amplifying said input signal; and

an amplitude identifying circuit for detecting the presence or absence of a burst signal in said input signal in said input signal based on the output signal from the DC variation removing signal amplifier;

said amplitude identifying circuit including:

an amplitude detection circuit for detecting the maximum amplitude of the output signal of said DC variation removing amplifier;

a threshold level control circuit for controlling the threshold level; and

a comparator circuit for comparing the output level of said amplitude detection circuit with said threshold level and outputting a detection signal indicating the presence or absence of the burst signal.

29. The burst signal detection circuit according to claim 28, wherein said DC variation removing signal amplifier includes:

a bottom detection circuit or a peak detection circuit for detecting the DC level variation of said input signal; and

an amplifier supplied with said input signal and the output signal of said bottom detection circuit or said peak detection circuit;

the negative phase output of said amplifier being fed back to the positive phase input side of said amplifier through a feedback resistor; and

the positive phase output of said amplifier being fed back to the negative phase input side of said amplifier through said peak detection circuit and a feedback resistor.

30. A burst signal detection circuit according to claim 28, wherein said DC variation removing signal amplifier includes a master-slave type automatic threshold control circuit having:

a master bottom detection circuit or a

master peak detection circuit for detecting the absolute minimum level or the absolute maximum level, respectively, of said input signal;

5 a slave peak detection circuit or a slave bottom detection circuit for detecting the relative maximum level or the relative minimum level, respectively, of said input signal from the output signal of said master bottom detection circuit or said master peak detection circuit; and

10 a voltage dividing circuit for generating a threshold level by dividing the output signal of said master bottom detection circuit or said master peak detection circuit and the output signal of said slave peak detection circuit or said slave bottom detection circuit.

31. The burst signal detection circuit according to claim 28, wherein said DC variation removing signal amplifier includes a master-slave type automatic threshold control circuit having:

20 a master bottom detection circuit or a master peak detection circuit for detecting the absolute minimum level or the absolute maximum level, respectively, of said input signal;

25 a voltage dividing circuit for generating a voltage divided signal by dividing the output signal of said master bottom detecting signal or said master peak detecting signal and said input signal; and

30 a slave peak detection circuit or a slave bottom detection circuit for generating a threshold level by detecting the relative maximum level or the relative minimum level, respectively, of said voltage divided signal from the output signal of said master bottom detection circuit or said master peak detection circuit.

35 32. The burst signal detection circuit according to claim 30, wherein the level hold capacitor of said slave peak detection circuit or said slave bottom detection circuit of said master-slave automatic threshold control

circuit is connected to the output of said master bottom detection circuit or said master peak detection circuit.

33. The burst signal detection circuit according to claim 31, wherein the level hold capacitor of said slave peak detection circuit or said slave bottom detection circuit of said master-slave automatic threshold control circuit is connected to the output of said master bottom detection circuit or said master peak detection circuit.

34. The burst signal detection circuit according to claim 28, wherein said amplitude identifying circuit includes:

a peak detection circuit or a bottom detection circuit for detecting the maximum level or the minimum level, respectively, of the output-single from the DC variation removing circuit;

a threshold level control circuit for generating a threshold level; and

a comparator circuit for comparing the output level of said peak detection circuit or said bottom detection circuit with said threshold level.

35. The burst signal detection circuit according to claim 28, wherein said amplitude identifying circuit includes a peak detection circuit or a bottom detection circuit for detecting the maximum level or the minimum level, respectively, of the output signal from the DC variation removing circuit, a threshold level control circuit for generating a threshold level by shifting the output level of said bottom detection circuit or said peak detection circuit by a predetermined value; and

a comparator circuit for comparing the output level of said peak detection circuit or said bottom detection circuit with said threshold level.

36. The burst signal detection circuit according to claim 28, wherein said amplitude identifying circuit includes:

a peak detection circuit and a bottom detection circuit for detecting the maximum level and the

minimum level, respectively, of the output signal from the DC variation removing circuit, a threshold level control circuit for generating a first threshold level by shifting the output level of said bottom detection circuit by a predetermined value and generating a second threshold level by shifting the output level of said peak detection circuit by a predetermined value; and

a comparator circuit for comparing said first threshold level and said second threshold level with each other.

37. The burst signal detection circuit according to claim 28, wherein said threshold level control circuit includes a temperature compensating circuit for changing said threshold level in accordance with the temperature change, said temperature compensating circuit being so configured as to compensate for the variation of the gain due to the temperature change.

38. The burst signal detection circuit according to claim 28, wherein said threshold level control circuit includes a reference voltage circuit for changing said threshold level with the supply voltage change, said reference voltage circuit being so configured as to compensate for the variation of the gain due to the supply voltage change.

39. The burst signal detection circuit according to claim 28, further comprising a photo-diode for receiving an optical signal and a preamplifier for converting the current signal from said photo-diode into a voltage signal, wherein the arrival of a burst signal is detected from the output signal of said preamplifier.

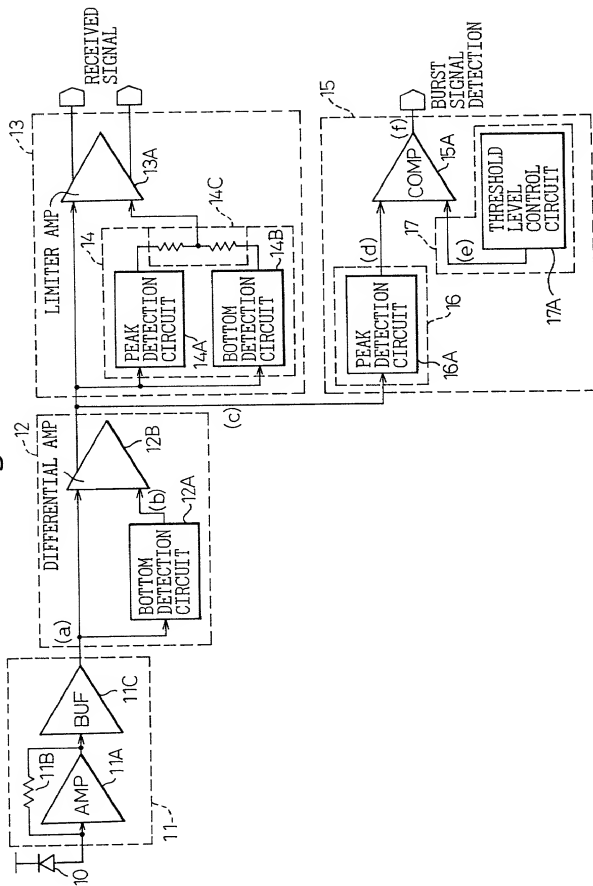
BURST SIGNAL DETECTION CIRCUIT

5

ABSTRACT OF THE DISCLOSURE

10 A burst signal detection circuit for detecting the  
arrival of a burst-like signal, which can accurately  
detect the burst signal against the DC level variations  
even in the case where the arriving burst signal is a  
weak signal, is disclosed. A DC variation removing  
circuit detects the bottom level of an input signal and  
removes the DC level variation of the input signal based  
15 on the bottom level. An amplitude identifying circuit  
detects the presence or absence of a burst signal based  
on the output signal of the DC variation removing  
circuit. The amplitude identifying circuit includes an  
amplitude detection circuit for detecting the maximum  
20 amplitude of the output signal of the DC variation  
removing circuit, a threshold level control circuit for  
controlling the threshold level and a comparator for  
comparing the output level of the amplitude detection  
circuit with the threshold level and outputting a  
25 detection signal indicating the presence or absence of a  
burst signal.

Fig.1





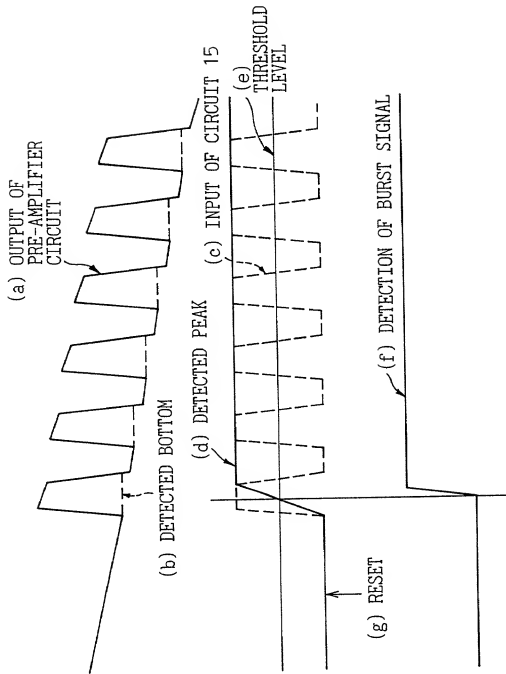


Fig.2A WAVEFORM IN  
CIRCUIT 12

Fig.2B WAVEFORM IN  
CIRCUIT 15

Fig.2C OUTPUT OF  
COMP 15A

Fig.3A

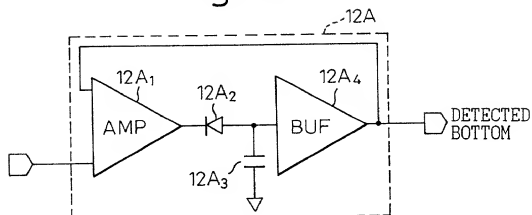


Fig.3B

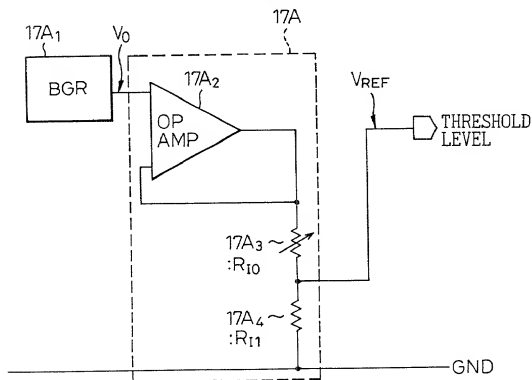
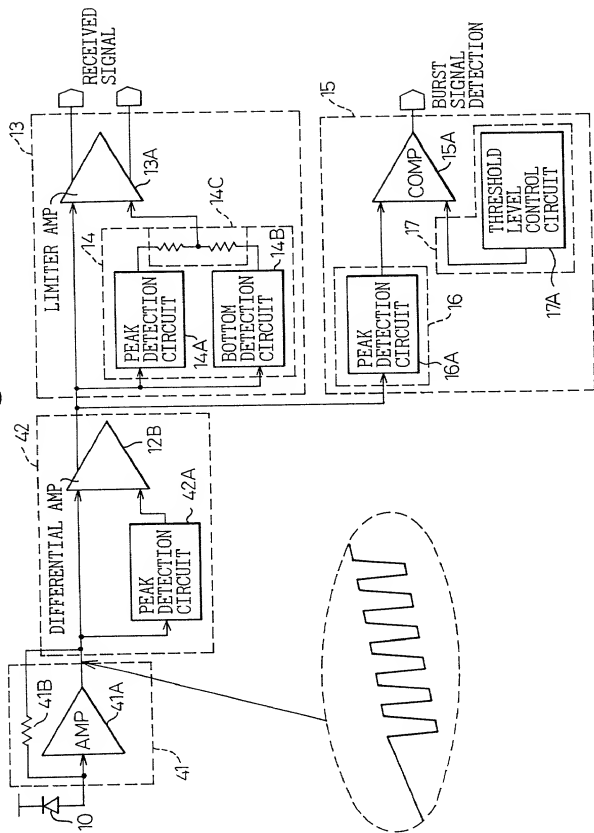


Fig. 4



The diagram illustrates a multi-stage signal processing circuit. It begins with a PDI input (10) connected to a diode (11A) and a buffer (11B). The signal then passes through an amplifier (11C) and a feedback loop (11A). The output of this stage is connected to a differential amplifier (12A) which includes a current source (12B) and a resistor (12C). The output of the differential amplifier is connected to a peak detection circuit (13A) and a bottom detection circuit (13B). The output of the peak detection circuit is connected to a limiter amplifier (13C). The output of the limiter amplifier is connected to a burst signal detection circuit (14A) which includes a resistor (14B) and a current source (14C). The output of the burst signal detection circuit is connected to a peak detection circuit (15A) and a bottom detection circuit (15B). The output of the peak detection circuit is connected to a comparator (15C) which includes a reference voltage (15D) and a threshold level control circuit (15E). The output of the comparator is connected to a burst signal detection circuit (15F) which includes a resistor (15G) and a current source (15H).

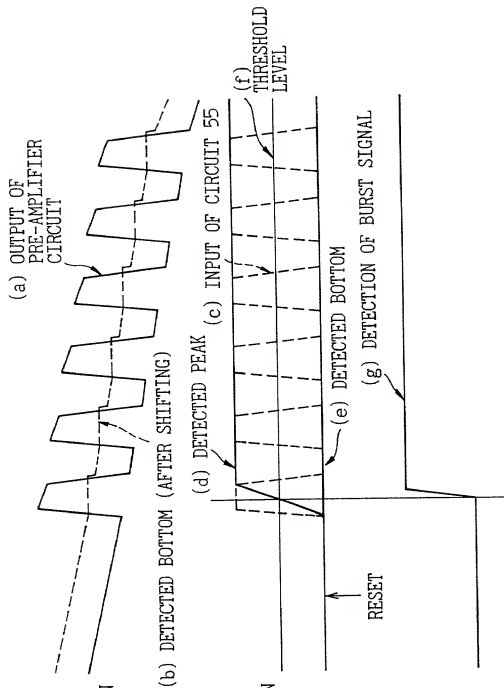


Fig. 6A WAVEFORM IN CIRCUIT 52

Fig. 6B WAVEFORM IN CIRCUIT 55

Fig. 6C OUTPUT OF COMP 15A

Fig.7

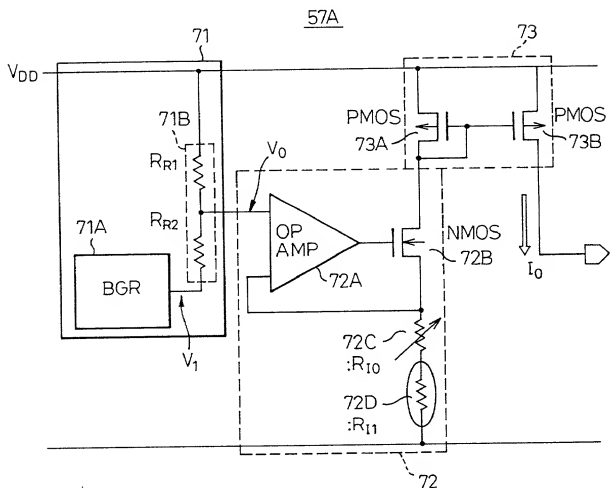


Fig.8

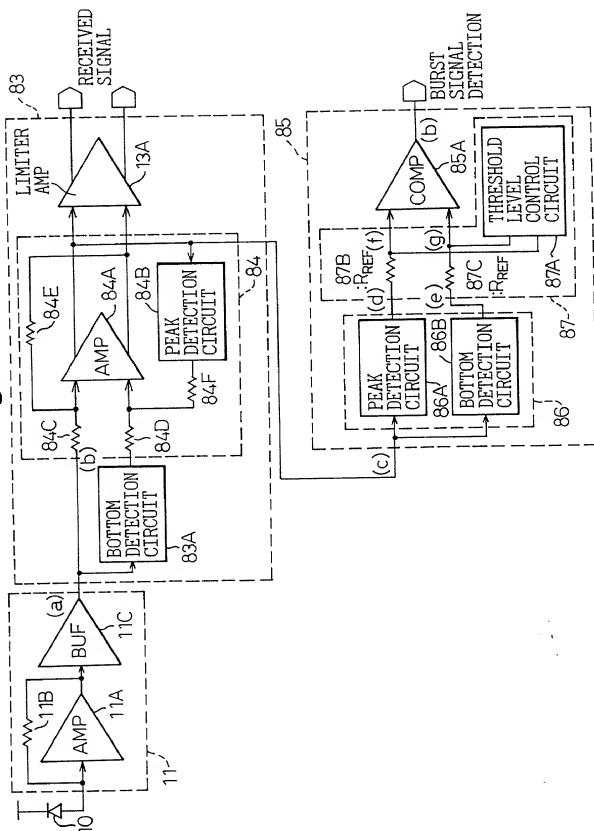


Fig.9A WAVEFORM IN  
CIRCUIT 83

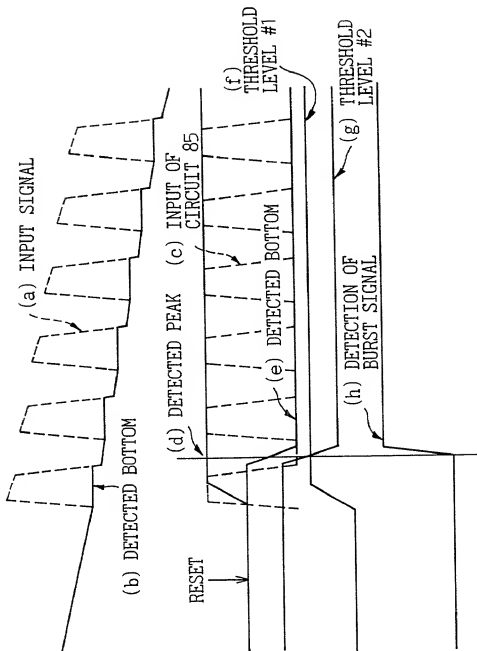


Fig.9B WAVEFORM IN  
CIRCUIT 85

Fig.9C OUTPUT OF  
COMP 85A



Fig.10A

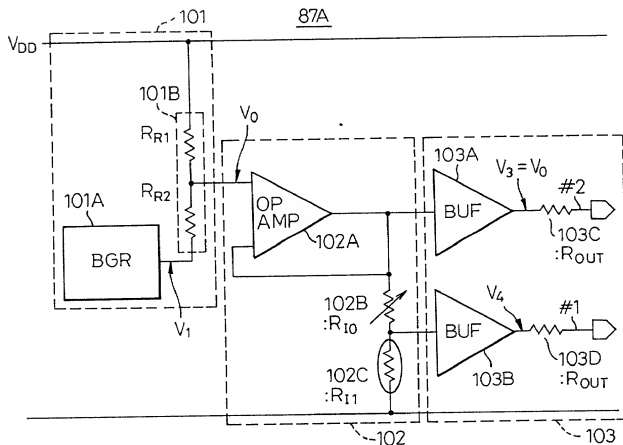


Fig.10B

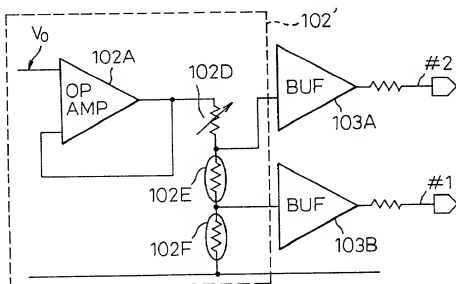
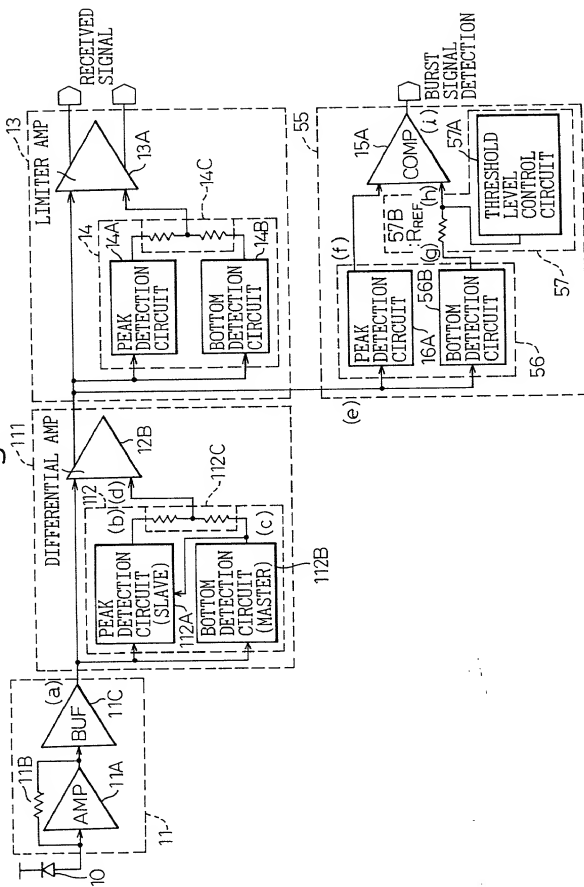


Fig.11



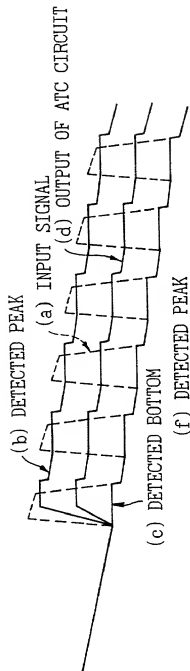


Fig.12A WAVEFORM IN  
CIRCUIT 111

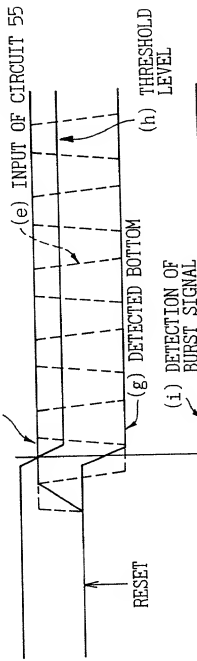


Fig.12B WAVEFORM IN  
CIRCUIT 55

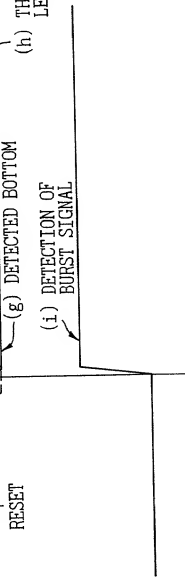


Fig.12C OUTPUT OF  
COMP 15A

Fig.13

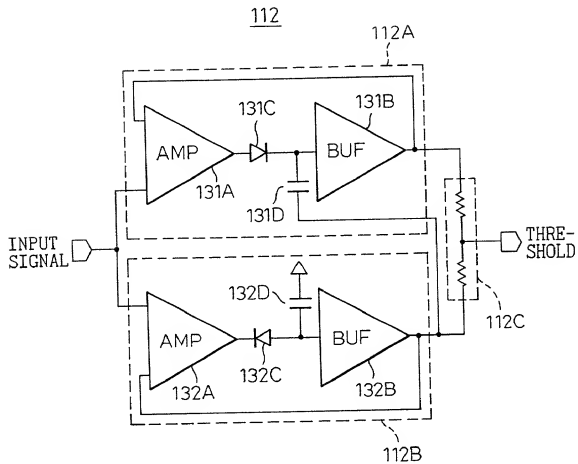


Fig.14

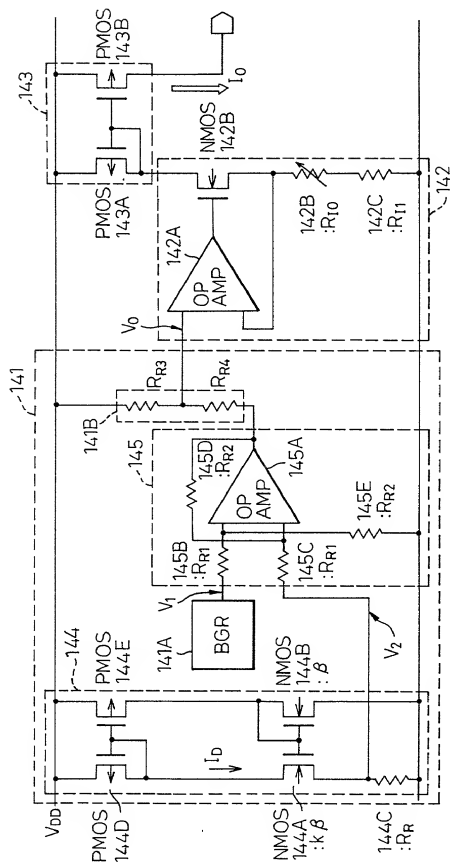


Fig.15

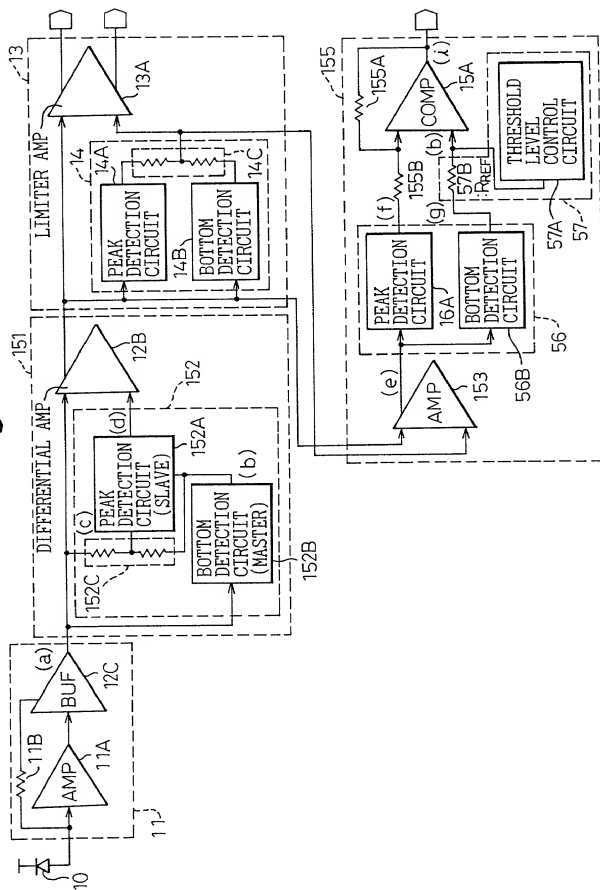


Fig.16A

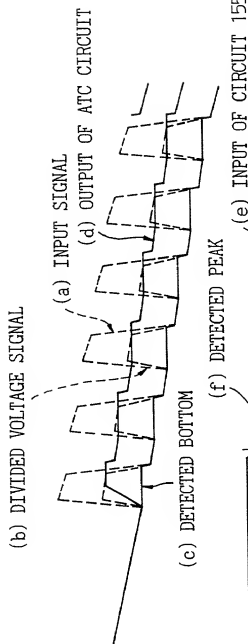


Fig.16B

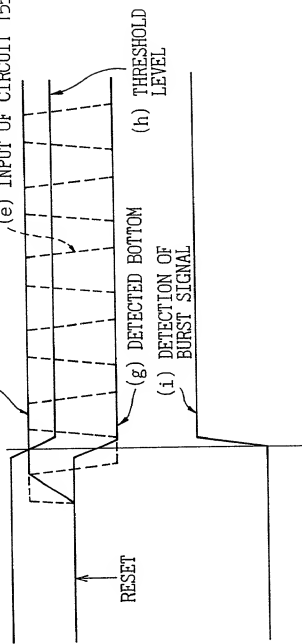


Fig.16C

OUTPUT OF  
COMP 15A

Fig.17

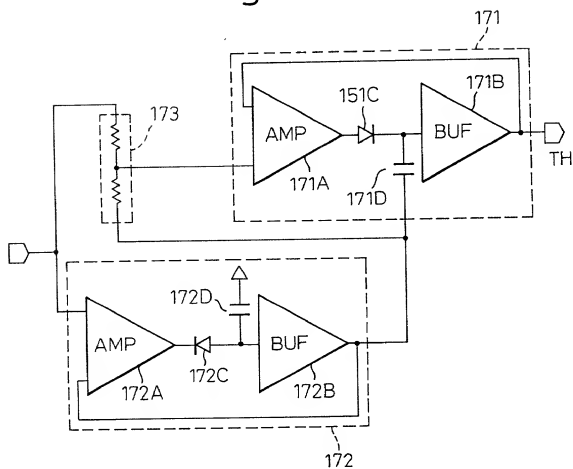




Fig. 18

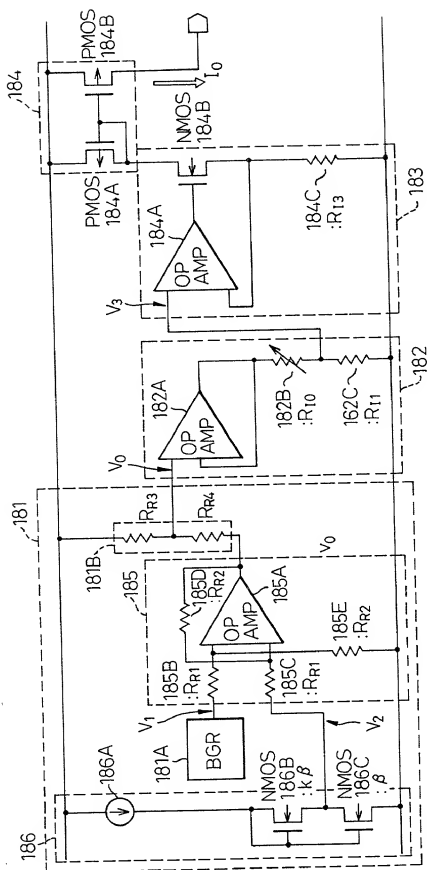
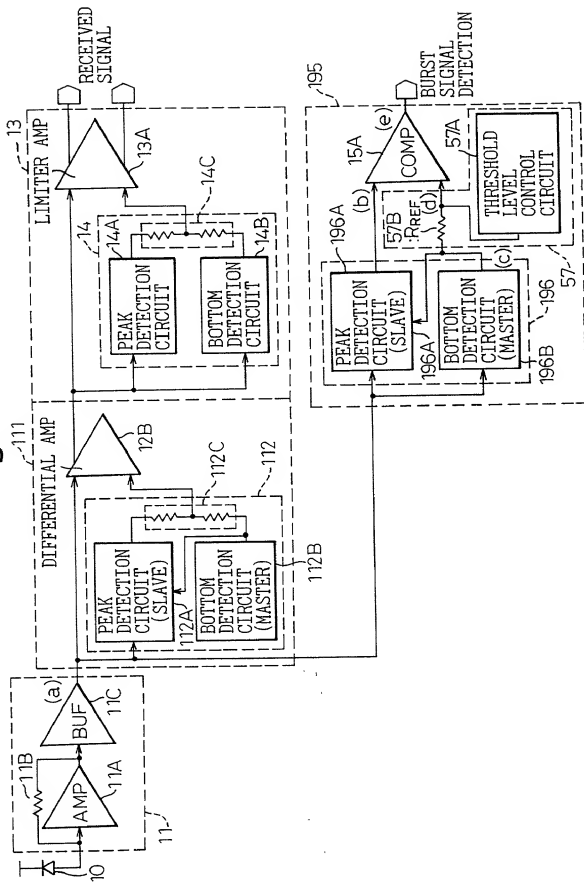


Fig.19



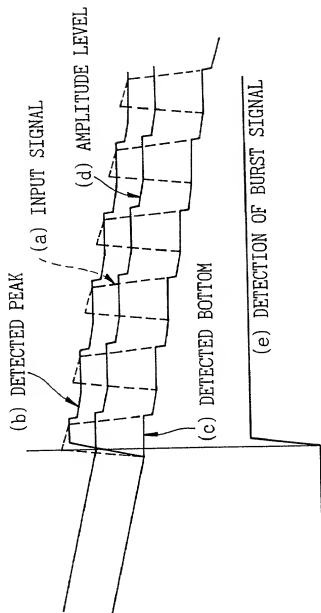


Fig.20A WAVEFORM IN  
CIRCUIT 195

Fig.20B OUTPUT OF  
COMP 15A



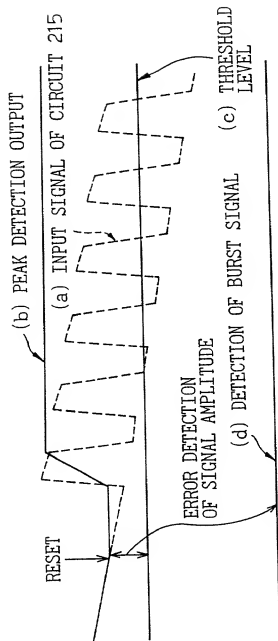


Fig.22A  
WAVEFORM IN  
CIRCUIT 215  
PRIOR ART

Fig.22B  
OUTPUT OF  
COMP 215A  
PRIOR ART

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Fig.23A

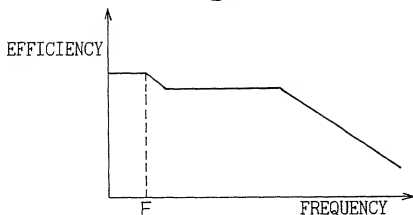


Fig.23B

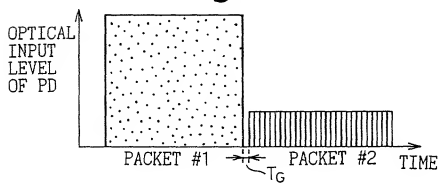
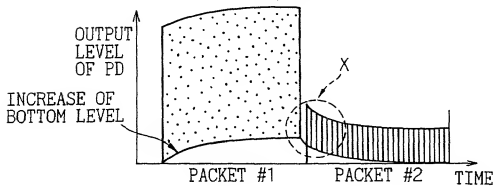


Fig.23C



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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

BURST SIGNAL DETECTION CIRCUIT

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as United States Application Number or  
PCT International Application Number  
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\_\_\_\_\_ (if applicable).

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## Prior Foreign Application(s)

外国での先行出願

11-062290 (Pat. Appln.)	Japan
(Number) (番号)	(Country) (国名)
(Number) (番号)	(Country) (国名)

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(Application No.) (出願番号)	(Filing Date) (出願日)
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(Application No.) (出願番号)	(Filing Date) (出願日)
(Application No.) (出願番号)	(Filing Date) (出願日)

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Priority Not Claimed  
優先権主張なし

9/March/1999
(Day/Month/Year Filed) (出願年月日)
(Day/Month/Year Filed) (出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)
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(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)
(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

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として、下記の者を指名いたします。(弁護士、または代理  
人の氏名及び登録番号を明記のこと)

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the following attorney(s) and/or agent(s) to prosecute this  
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THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Satoshi IDE et al.**

Filed: : **Concurrently herewith**

For : **BURST SIGNAL DETECTION CIRCUIT**

Serial No.: **Concurrently herewith**

January 6, 2000

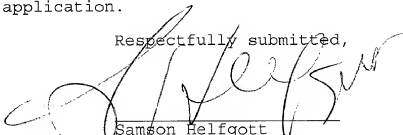
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SUB-POWER OF ATTORNEY

S I R:

I, Samson Helfgott, Reg. No. 23,072 attorney of record  
herein, do hereby grant a sub-power of attorney to Linda S.  
Chan, Reg. No. 42,400, Jacqueline M. Steady, Reg. No., 44,354  
and Harris A. Wolin, Reg. No. 39,432 to act and sign in my behalf  
in the above-referenced application.

Respectfully submitted,



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DOCKET NO.: FUJA16.923  
LHH:power

Filed Via Express Mail

Rec. No. EL522353992US

On: January 6, 2000

By L. Karas

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